**ALU VERIFICATION PLAN**

**1. Project Overview**

This verification plan targets an Arithmetic Logic Unit (ALU) design capable of performing a variety of arithmetic and logical operations. It supports:

* Two operands (OPA, OPB)
* A command code (CMD)
* A mode signal (MODE) to switch between arithmetic (1) and logic (0)
* Input validity flags (INP\_VALID)
* Clock enable (CE)
* Carry-in (CIN)
* Output result and status flags (COUT, OFLOW, G, L, E, ERR)

The ALU also has specific behavior such as:

* Waiting 16 clock cycles for the second operand if only one is valid
* Error signaling for invalid rotate commands or timeout

**2. Verification Objectives**

* Verify correct functionality of all ALU operations across both arithmetic and logical modes by comparing DUT output with expected values.
* Ensure output flags (G, L, E, COUT, OFLOW, ERR) are set correctly under relevant conditions and commands.
* Validate reset functionality by confirming all outputs are cleared when RST is asserted, regardless of current or past inputs.
* Check for correct 16-clock wait behavior when only operand A is valid (INP\_VALID = 2’b01), triggering ERR if operand B is not received within 16 cycles.
* Achieve 100% functional and cross coverage by sampling all meaningful combinations of inputs such as CMD, MODE, CIN, INP\_VALID, and control signals.
* Assert timing and protocol correctness using assertions, ensuring proper sequencing of signals, stable control signals, and correct response to invalid or boundary inputs.

**3. DUT Interfaces**

| **Signal** | **Direction** | **Bit-width** | **Description** |
| --- | --- | --- | --- |
| OPA | Input | [WIDTH-1:0] | Operand A |
| OPB | Input | [WIDTH-1:0] | Operand B |
| CIN | Input | 1 bit | Carry-in |
| CMD | Input | [CMD\_WIDTH-1:0] | ALU operation command (0–13) |
| MODE | Input | 1 bit | 1 = Arithmetic mode, 0 = Logical mode |
| INP\_VALID | Input | 2 bits | Operand validity: bit[0] for OPA, bit[1] for OPB |
| CE | Input | 1 bit | Clock Enable |
| CLK | Input | 1 bit | Clock |
| RST | Input | 1 bit | Asynchronous Reset |
| RES | Output | [RES\_WIDTH-1:0] | Result of the ALU operation |
| COUT | Output | 1 bit | Carry-out |
| OFLOW | Output | 1 bit | Overflow flag |
| G | Output | 1 bit | Greater-than flag from CMP |
| L | Output | 1 bit | Less-than flag from CMP |
| E | Output | 1 bit | Equal-to flag from CMP |
| ERR | Output | 1 bit | Error flag (bad rotate or 16-cycle timeout) |

**4. Testbench Architecture**

1. Top Module

* Purpose: Integrates the DUT and connects it to the verification environment using the virtual interface.
* Details:
  + Instantiates the ALU DUT and interface
  + Passes the virtual interface to the test
  + Launches simulation by calling the start() or run() method in the test

2. Test Class

* Purpose: Acts as the main test trigger.
* Details:
  + Creates and configures the environment
  + Starts all component processes (generator, driver, etc.)
  + Runs one or more test scenarios

3. Environment

* Purpose: Encapsulates all sub-components and connects them.
* Details:
  + Instantiates generator, driver, monitor, reference model, scoreboard
  + Sets up communication between them using mailboxes to transfer transactions
  + Coordinates the simulation flow

4. Generator

* Purpose: Produces random or constrained-random input stimulus.
* Details:
  + Generates transactions with randomized inputs like opa, opb, cmd, etc.
  + Sends these transactions to the driver for actual application to the DUT

5. Driver

* Purpose: Drives the input values onto the DUT.
* Details:
  + Retrieves input transactions from the generator
  + Applies the transaction fields to the DUT through the interface
  + Also passes the transaction to the reference model for expected output computation
  + Samples functional coverage for all input stimuli

6. Monitor

* Purpose: Passively observes DUT signal activity.
* Details:
  + Collects DUT output and relevant input values into a transaction
  + Sends this data to the scoreboard
  + Useful for coverage sampling and debug

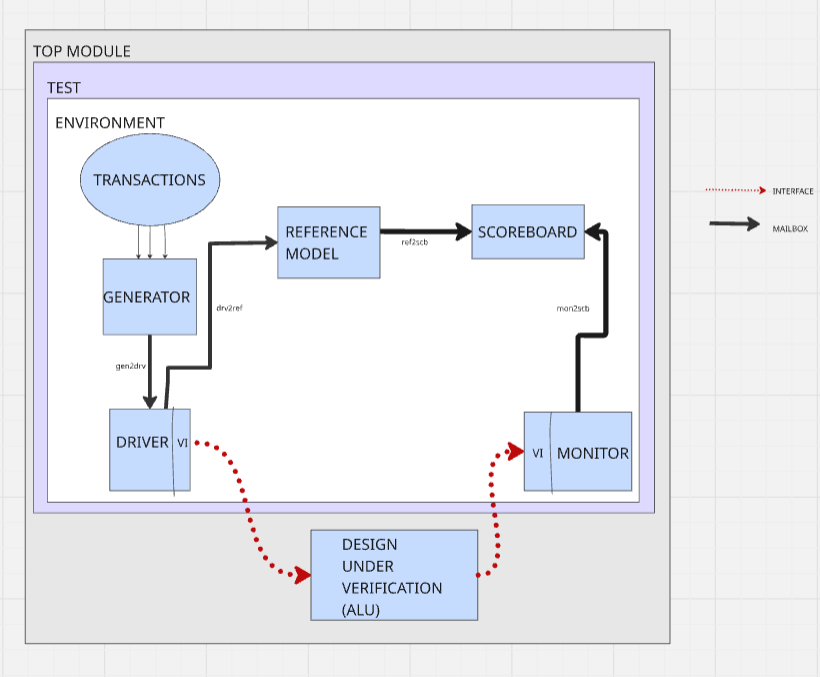
7. Reference Model

* Purpose: Models the correct behavior of the ALU.
* Details:
  + Receives input transactions from the driver
  + Computes expected outputs based on ALU functionality
  + Sends these computed values to the scoreboard for comparison

8. Scoreboard

* Purpose: Validates DUT output correctness.
* Details:
  + Receives actual output from the monitor and expected output from the reference model
  + Compares each field (e.g., res, cout, g/l/e, err)
  + Reports mismatches for debugging and coverage tracking

**Diagram**



**5. Test Plan**

**Test Scenarios**

* Apply all 14 ALU commands with a range of operands in both arithmetic and logical modes.
* Verify all input combinations of INP\_VALID including valid/invalid operand cases.
* Test with CIN set to 0 and 1 during ADD\_CIN and SUB\_CIN.
* Check behavior when CE is deasserted (no operation should take place).
* Apply edge cases such as maximum and minimum operand values (e.g., 0, mid-range, max).
* Confirm correct G, L, E flags when CMD\_CMP, CMD\_SIGN\_ADD, and CMD\_SIGN\_SUB are used.
* Trigger error condition by providing OPA only and delaying OPB beyond 16 clock cycles.
* Trigger error by giving invalid rotate values (non-zero bits in OPB[WIDTH-1:SHIFT+1]).
* Assert reset at various stages to check proper reset response.
* Confirm behavior when illegal combinations (like invalid CMD) are input.

**Functional Coverage Plan**

* CMD\_CP: Cover all 14 ALU commands.
* MODE\_CP: Cover both logical and arithmetic modes.
* INP\_VALID\_CP: Cover all operand validity combinations (00, 01, 10, 11).
* CE\_CP: Cover CE being 0 and 1 during operation.
* CIN\_CP: Test CIN = 0 and 1 for ADD\_CIN/SUB\_CIN commands.
* OPA\_CP and OPB\_CP: Cover operand edge values (e.g., 0, mid, max).
* RST\_CP: Test reset condition clearing the outputs.
* ERR\_CP: Cover both error and no-error scenarios (rotate and timeout).
* CMP\_OUT\_CP: Ensure CMP command sets correct G, L, E flags.

**Cross Coverage:**

* CMD × MODE
* CMD × INP\_VALID
* CMD × ERR
* CMD × CMP Output Flags
* CMD × Wait-16 behavior

**Assertions**

* CMD signal must remain stable when CE is low.
* ERR must never be asserted during valid input and legal command conditions.
* When RST is high, all outputs must reset to default.
* If INP\_VALID is 2'b01, a timer must count 16 clock cycles waiting for OPB; if not received, ERR must go high.
* During rotate operations (CMD = 12 or 13 in logical mode), if OPB[WIDTH-1:SHIFT+1] != 0, then ERR must assert.
* RES and flags must only update on the rising edge of CLK when CE is high and inputs are valid.